REMARKS

Claims 55-83 are all the claims pending in the application. Claims 1-54 are cancelled and new claims 55-83 are added, above. Previous claims 1-54 stood rejected on informalities and prior art grounds. The cancellation of the rejected claims renders the rejections moot; however, many of the same features are claimed in the newly added claims and some distinctions between the claimed invention and the applied references is included below. In addition, the drawings and specification are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. The Objections to the Drawings and Specification

With respect to paragraph 2.0 of the Office Action, the specification has been amended to change the description to refer to Figure 4A. With respect to paragraph 3.0 of the Office Action, the proposed drawing corrections submitted herewith remove reference character 38. Further, the specification has been amended to indicate that reference character 49 is shown in Figure 5. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 1, 22, 25, 31, 33, 37, 43, 47, and 49 stand rejected under 35 U.S.C. §102(b) as being anticipated by Paterson (U.S. Patent No. 5,566,186). Claims 2, 3, 10, 20, 26-27, 42, and 52-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Bencivenga (U.S. Patent No. 5,341,314). Claims 4 and 5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Bencivenga, and further in view of Hii (U.S. Patent No. 6,353,563). Claims 8, 9, and 18 stand rejected under 35 U.S.C. §103(a) as being

unpatentable over Paterson in view of Bencivenga, and further in view of Collins (U.S. Patent No. 3,651,315). Claims 11-14, 21, 23, and 54 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Bencivenga, and further in view of Franke (U.S. Patent No. 4,122,995). Claims 16 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Bencivenga, and further in view of Stoner (U.S. Patent No. 4,768,195). Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Bencivenga, and further in view of Graef (U.S. Patent No. 6,037,7960). Claim 30 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Collins. Claims 32 and 38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Hii. Claims 28, 39, and 44-46 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view Franke. Claims 29 and 48 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson. Claims 35 and 50 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Tallman (U.S. Patent No. 4,773,028). Claims 36 and 51 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Paterson in view of Stoner. As mentioned above, the cancellation of claims 1-54 renders such rejections moot. However, a discussion of many distinctions between the claimed invention and the applied references is included below.

A. The Paterson Reference

Newly added claims 55 and 63 define a "transportable integrated circuit chip test device" that is not taught or suggested by any of the prior art of record. Paragraph 9.0 of the Office Action proposes that Patterson teaches a method for testing integrated circuit chips that can be implemented during transport and refers to column 1, lines 32-39 of Paterson to support this proposition. While Patterson is silent regarding any transportability of its testing device, the Office Action proposes that conducting the test during transport will merely change the environment in which the test is being conducted and will not require any changes to the testing circuit. Applicants strongly disagree with this conclusion.

Initially, Applicants note that none of the prior art of record teaches or suggests a portable testing device, a much less one that is defined by independent claims 55 and 63 that can test the integrated circuit chips while they are being transported. There is no direct teaching (much less any suggestion) in any of the prior art of record for testing chips while they are being transported. The unsupported statements in the Office Action that testing during transport will merely change the environment in which the test is being conducted is an interesting supposition; however, it is completely unsupported by any of the prior art record. To the contrary, the source of such reasoning is clearly based upon hindsight, in that the only document in this application which suggests such a structure is Applicants' disclosure. In order for Applicants' claimed invention to be anticipated or obvious in view of the prior art requires some teaching (or least some suggestion) from the prior art of record that one ordinarily skilled in the art would have been motivated to arrive at the claimed invention. In this instance, there is no art that in any way suggests that testing of integrated circuit chips should be performed while the chips are being transported.

With the claimed invention, after the chips are manufactured in the foundry, they could be mounted on test board 11 and tested during transportation (e.g., on the way to the system house). The chips which were determined to be good, would be removed for assembly, while chips which were determined to be bad could be returned to the foundry (or some other location) in in-transit box 20. This would allow diagnostics to be performed to determine the source of the defect. Since there is simply no support in the prior record for a transportable integrated circuit chip test device, Applicants respectfully submit that Patterson does not teach or suggest the invention defined by independent claims 55 and 63.

B. The Bencivenga Reference

Independent claims 71 and 78 define that the "testing circuitry identifies a defective integrated circuit chip as one having a different output when compared to outputs of the other integrated circuit chips." The Office Action (in paragraph 16.1) admits that Patterson does not

teach this limitation but argues that Bencivenga in column 1, lines 65-column 2, line 14 teaches a testing circuit for comparing the output signals with each other in response to test patterns. Applicants respectfully disagree with the interpretation of Bencivenga in the Office Action.

Applicants note that in column 1, lines 7-10, Bencivenga is directed to a method of generating test vectors and that the portion of Bencivenga referred to in paragraph 16.1 of the Office Action is a detailed explanation of how the vectors are generated. Bencivenga does not disclose the claimed structure that identifies defective integrated circuit chips as those having a different output when compared to all other integrated circuit chips. Thus, Applicants submit that Bencivenga does not teach what it is purported to teach in paragraph 16.1 of the Office Action.

The claimed invention provides a substantially simplified system for testing chips because the invention does not need to know the output a given input should produce. This is especially important in ASIC chip testing because each different design of ASIC chips has a potentially different output for a given input. Each batch of ASIC chips has potentially different performance parameters from other batches of ASIC chips. This presents special testing problems to conventional systems, because the proper output for each different batch of ASIC chips must be known before the chips can be properly tested. However, with the invention since the chips are merely tested against other chips in the same batch to determine if similar output signals are produced, the invention does not need to know the specific output a given input should produce. This is true whether the chips are tested against other untested neighboring chips or also tested against a known good golden chip.

Thus, as shown above, Bencivenga does not disclose that the "testing circuitry identifies a defective integrated circuit chip as one having a different output when compared to outputs of the other integrated circuit chips" as defined by independent claims 71 and 78 but instead merely discloses a method of generating test vectors. Therefore, Bencivenga cannot properly be used in combination with any other prior art of record to teach this claimed feature and Applicants submit that this, along with other claimed features, makes independent claims 71 and 78 patentable over the prior art of record.

C. The Hii Reference

Hii discloses an integrated circuit that has a built-in self-test (BIST) arrangement (60). The built-in self-test arrangement includes a read only memory (ROM), (140) that stores test algorithm instructions. A ROM logic circuit (410) receives an instruction read from the read only memory and produces a group of output signals dependent upon the instruction. A BIST register 420 receives and stores the group of output signals from the logic circuit for controlling self-test of the integrated circuit.

Hii is referenced for the limited purpose of teaching that a BIST engine was well known at the time of the invention. The present claims that do not define a BIST engine. Therefore, Hii is irrelevant to the claimed invention.

D. The Collins Reference

Collins discloses a digital product inspection system using a digital pseudorandom generator in combination with a characteristic of the product being inspected to produce a unique set of data combinations which when compared with previously taken data from the test of a know good unit will provide an output indicating whether or not the characteristic of the unit under test is within acceptable limits.

Collins is referenced for the limited purpose of teaching a power supply to stress the chips under test. While it is undoubtedly necessary to have a power supply to perform any form of testing, Applicants note that the claimed structure define that the power supply is a "portable power supply" (independent claims 55 and 63). The power supply mentioned in Collins is not portable and there is no mention in Collins regarding the portability of the power supply. Applicants further note that dependent claims 57 and 66 define that the portable power supply is a battery. Collins is clearly deficient in teaching these aspects of the claimed invention.

Therefore, any combination of Collins with the remaining prior art of record would not teach or suggest the invention as defined by independent claims 55 and 63.

E. The Franke Reference

Franke discloses an improved means and method for continuously and asynchronously testing the operation of a digital circuit or unit. The testing approach is based on determining whether an output signal from the unit under test is out of skew with a corresponding output from a standard unit for at least an adjustable predetermined minimum time period. Franke is referenced for the limited purpose of teaching an XNOR tracking circuit. The present claims do not define an XNOR device and, therefore, Franke is irrelevant to the claimed invention.

F. The Stoner Reference

Stoner discloses a chip tester for testing microelectronic circuit chips. The tester is capable of testing a variety of chip types in a single socket, including chips having different circuit functions, different pin configurations, and different number of pins. Tests are performed without any preliminary tester setup steps other than placing the chip to be tested into the test socket. The tester applies input voltages and output loads and monitors input and output signals for a first possible chip type, and upon failing to meet expected input/output measurement conditions, applies input voltages and output loads and monitors input and output signals for a second possible chip type. The process is repeated and continues until the monitored inputs/outputs for the chip under test meet the expected input/output measurement conditions, at which time a display device indicates that the chip under test is operational and, preferably, displays the chip type. The tester then repeatedly applies the test procedure only for the chip type being tested, the latter test procedure repeating indefinitely. The inputs and outputs continue to be monitored, and should an error appear in the measurements during any of the repeated tests, a

count is made of the number of errors detected, and the count of the number of errors is displayed.

Stoner is referenced as teaching a visible indicator. Dependent claims 56, 65, 73, and 80 define a structure that includes visual test failure indicators where "one of said visual test failure indicators is adjacent each of said sockets." The claimed structure is fundamentally different than the structure disclosed in Stoner because Stoner only discloses a display 13 that counts the number of errors and does not disclose a visual indicator that is adjacent sockets that hold chips being tested where the visual indicator denotes the location of a defective chip. To the contrary, the visual indicator (display 13) disclosed in Stoner is not positionally located to indicate a failure, but instead merely discloses the number of errors. In other words, with the claimed invention, the position of the defective chip is readily identified, while with the structure disclosed in Stoner, such a position is not identified by the visual test indicators. Therefore, if Stoner had been combined with any other prior art of record, it would not teach or suggest the structure defined by dependent claims 56, 65, 73, and 80.

G. The Graef Reference

Graef discloses a method of testing a semiconductor device that includes generating a current waveform for the semiconductor device by measuring the response of the device to an initializing vector group and comparing the current waveform to a golden waveform to determine whether the semiconductor device is good or defective. An apparatus for testing the semiconductor device includes a vector generator providing an initialization vector group to the semiconductor device, a measurement unit for measuring a plurality of current measurements from the semiconductor device which responds to the input of the initialization vector group, a generation unit for generating a current waveform from the current measurements of the semiconductor device, and an analysis unit for comparing the current waveform to a golden waveform to determine whether the device falls outside a tolerance margin of the golden waveform.

The Office Action proposes that Graef discloses the use of sockets to hold chips being tested. However, Applicants note that none of the prior art of record teach or suggest the use of sockets in a testing device that includes the structure defined by independent claims 55, 63, 71, and 78. For example, such claims define a "portable box" (claims 55 and 63), testing circuitry included directly upon the board on which the sockets are placed (claims 71 and 78), as well as other similar features. Such structures defined by Applicants' independent claims have never been used with sockets in testing devices previously.

The Examiner's conclusions (in paragraph 37.1 of the Office Action) that it would have been obvious to place such components on a single board and that the placement of such components on a single board would not affect the function of the tester are not supported by any teaching in the prior art of record. Instead, such reasoning is clearly based upon hindsight analysis in light of the teachings in Applicants' disclosure. To the contrary, all the testing devices disclosed prior art of record require that the majority of logic testing is performed outside the board to which the chips are connected. Therefore, including such devices on a single board would actually destroy the function of the devices described in the prior art of record.

All references which disclose a "golden chip" disclose that this golden chip is utilized exterior to the board to which any such chips being tested are connected. The invention breaks away from such conventional teachings and includes such a "golden chip" directly attached to each board to which the chips are connected using the sockets. There is simply no motivation in the prior art of record to do what Applicants have done and the conclusions reached in the Office Action are completely unsupported and, therefore, clearly based upon hindsight reasoning, which is improper. Thus, any combination of references that includes Graef would not teach or suggest the invention as defined by independent claims 55, 63, 71, and 80.

H. The Tallman Reference

Tallman discloses a method and apparatus for the improved monitoring and detection of improper device operation. Operation of a prototype device is first modeled. In particular, a set

of test vectors is selected to provide a desired degree of testing of the prototype unit. The expected response of the prototype to the selected set of test vectors is determined through the use of analytical prediction means, and stored for subsequent comparison with the operation of the prototype unit. Thereafter, the selected set of test vectors are applied to the prototype unit, and the response thereto is compared in real time with the expected responses. Improper operation of the prototype device is thereby identified, and associate information recorded for subsequent analysis.

The Office Action proposes that the history data collection unit disclosed in Tallman teaches the claimed feature of "a memory adapted to store test results" as defined by new dependent claims 58, 67, 74, and 81. However, Tallman does not teach or suggest including a memory adapted to store test results in a testing device that includes the structure defined by independent claims 55, 63, 71, and 78. For example, such claims define a "portable box" (claims 55 and 63), testing circuitry included directly upon the board on which the memory device is placed (claims 71 and 78), as well as other similar features. Such structures find by Applicants' independent claims have never been used with the claimed memory in testing devices previously. Thus, any combination of references that includes Tallman would not teach or suggest the invention as defined by dependent claims 58, 67, 74, and 81 .

III. Conclusion

Applicants submit that the newly added claims are patentable over the prior art of record for the reasons indicated above and for other reasons not mentioned above. The features defined by the claims that are discussed above are only discussed because they are mentioned directly or indirectly in the Office Action. Many other patentable features are claimed, yet are not discussed above, principally because they were not mentioned in the Office Action.

Independent claims 55 and 63 define structures that allows integrated circuit chips to be tested while they are being transported. There is no teaching or suggestion of the structure (or

even this concept) in any of the prior art references. This structure is extremely valuable because it allows the chips to be tested during a time when they are otherwise idle (when they are being transported) and there is no suggestion in the prior art for doing this. This decreases testing time substantially and/or allows extensively more testing.

Independent claims 71 and 78 define a structure where the testing circuitry is included on the same board to which the chips are connected and which performs testing in such a way that it is not necessary to know what the tested chips should be outputting. To the contrary, the claimed structure identifies defective chips merely by determining if a chip produces an output that is different than the remaining chips. Again, this is extremely advantageous because it eliminates the conventional systems requirement of knowing what a specific chip should produce.

None of these features (or even the related concepts) are taught or suggested by the prior art of record and clearly no structure as defined by the claims is taught by the prior of record. Therefore, for these reasons, and for other reasons not mentioned herein, the newly added claims are patentable over the prior art of record.

In view of the foregoing, Applicants submit that claims 55-83, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 12/3/02

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Marked Up Version of Changes Made:

IN THE SPECIFICATION:

Page 7, lines 12-19, please replace with the following paragraph:

FIG. 4(a) illustrates more details about test stimuli generator 34 and control device 31 in FIG. 3. Test stimuli generator 34 is a source of test patterns, such as built in self test (BIST) engine 42 and seed patterns 43. Control device 31 includes MUX 40, exclusive NOR (XNOR) checker/comparator 41, golden chip 37, test control register (TCR) mask 48, and status indicator 44. BIST engine 42 uses the seed patterns 43 to produce the test stimuli. The number of XNOR checker/comparators 41a to 41m, is equal to the number of outputs m each chip has, as shown in FIG. 4b. Each XNOR checker/comparator 41a-41m, is n-way, where n is the number of sockets for holding chips to be tested.

Page 9, lines 12-18, please replace the paragraph as follows:

The TCR mask and status indicator 44 are written to keep MUX 40 of a defective chip connected to golden chip 37 through line 49 as described below in Figure 5. TCR 46 permanently selects golden chip data through that MUX 40 that was connected to the defective chip for the remaining portion of the test using output line 49 from TCR mask 48. From that point on, TCR mask 48 locks the status bit of the defective chip in the status indicator 44. In this manner, as each failing chip is identified, it is isolated, marked, removed from any further testing, and its data replaced by data from golden chip 37.